What is claimed is:

1. A level shift circuit for amplifying an input signal having a first amplitude to an output signal having a second amplitude, comprising:

a first inverter having a first input terminal and a first output terminal for generating the output signal, the first inverter including a first transistor having a first current driving capacity;

a second inverter having a second input terminal connected to the first output terminal and a second output terminal connected to the first input terminal, the second inverter including a second transistor having a second current driving capacity that is smaller than the first current driving capacity; and

an inversion circuit having a third output terminal connected to the first input terminal, the inversion circuit receiving the input signal including a first input signal and a second input signal, the inversion circuit including a third transistor having a third current driving capacity that is smaller than the first current driving capacity and is larger than the second driving capacity,

wherein one of the first and second input signals is a one-shot pulse signal.

2. A level shift circuit according to claim 1, wherein the first inverter includes a first NMOS transistor and a first PMOS transistor connected in

series and the second inverter includes a second NMOS transistor and a second PMOS transistor connected in series,

wherein gate terminals of the first NMOS and PMOS transistors are connected to the second and third output terminals, and

wherein the first output terminal is connected to gate terminals of the second NMOS and PMOS transistors.

3. A level shift circuit according to claim 1, wherein the inversion circuit has a third NMOS transistor and a third PMOS transistor connected in series.

4. A level shift circuit according to claim 3, wherein the first input signal is the one-shot pulse signal.

5. A level shift circuit according to claim 4, wherein the inversion circuit further includes a fourth transistor having a fourth current driving capacity that is substantially identical to the second current driving capacity, the fourth transistor being normally conductive, and an fifth transistor connected in series with the fourth transistor, the fifth transistor having a fifth current driving capacity that is substantially identical to the third current driving capacity, the fifth transistor receiving the first input signal, and

wherein the third PMOS transistor is driven by a signal outputted from a connecting portion of the fourth and fifth transistors.

6. A level shift circuit according to claim 2, wherein the second inverter further includes a sixth transistor having a current driving capacity that is substantially identical to the second current driving capacity, the sixth transistor weakening retention of a state of the second inverter where the state is inverted.

7. A level shift circuit according to claim 3, wherein said inversion circuit further includes a transistor which has a current driving capacity substantially identical to the second current driving capacity and is adapted to weaken retention of a state of a connecting portion of the fifth and sixth transistors where the state thereof is inverted.

8. A level shift circuit according to claim 1, further comprising a one-shot pulse generator for generating the one-shot pulse signal in response to the second input signal.

9. A level shift circuit according to claim 8, wherein the one-shot pulse generator generates a one-shot pulse signal in response to a delay signal generated from the second input signal.

10. A semiconductor integrated circuit amplifying an input signal having a first amplitude to an output signal having a second amplitude, the semiconductor integrated circuit comprising:

a first inverter having a first input terminal and a first output terminal for generating the output signal,

the first inverter including a first transistor having a first current driving capacity;

a second inverter having a second input terminal connected to the first output terminal and a second output terminal connected to the first input terminal, the second inverter including a second transistor having a second current driving capacity that is smaller than the first current driving capacity; and

an inversion circuit including a third transistor having a third current driving capacity that is smaller than the first current driving capacity and is larger than the second driving capacity, the inversion circuit driving the first inverter in response to the input signal, wherein the input signal includes a first input signal and a second input signal one of which is a one-shot pulse signal.

11. A level shift circuit according to claim 10, wherein the first transistor includes a first NMOS transistor and a first PMOS transistor connected in series and the second transistor includes a second NMOS transistor and a second PMOS transistor connected in series,

wherein gate terminals of the first NMOS and PMOS transistors are connected to the second output terminal and an output terminal of the inversion circuit, and

wherein the first output terminal is connected to gate terminals of the second NMOS and PMOS transistors.

12. A level shift circuit according to claim 10, wherein the third transistor has a third NMOS transistor and a third PMOS transistor connected in series.

13. A level shift circuit according to claim 12, wherein the first input signal is the one-shot pulse signal.

14. A level shift circuit according to claim 13, wherein the inversion circuit further includes a fourth transistor having a fourth current driving capacity that is substantially identical to the second current driving capacity, the fourth transistor being normally conductive, and an fifth transistor connected in series with the fourth transistor, the fifth transistor having a fifth current driving capacity that is substantially identical to the third current driving capacity, the fifth transistor receiving the first input signal, and

wherein the third PMOS transistor is driven by a signal outputted from a connecting portion of the fourth and fifth transistors.

15. A level shift circuit according to claim 11, wherein the second inverter further includes a sixth transistor having a current driving capacity that is substantially identical to the second current driving capacity, the sixth transistor weakening retention of a state of the second inverter where the state is inverted.

16. A level shift circuit according to claim 12, wherein said inversion circuit further includes a

transistor which has a current driving capacity substantially identical to the second current driving capacity and is adapted to weaken retention of a state of a connecting portion of the fifth and sixth transistors where the state thereof is inverted.

17. A level shift circuit according to claim 10, further comprising a one-shot pulse generator for generating the one-shot pulse signal in response to the second input signal.

18. A level shift circuit according to claim 17, wherein the one-shot pulse generator generates a one-shot pulse signal in response to a delay signal generated from the second input signal.

19. A level shift circuit comprising:

a first inverter having a first input terminal and a first output terminal for generating an output signal having a first amplitude, the first inverter including a first transistor having a first current driving capacity;

a second inverter having a second input terminal connected to the first output terminal and a second output terminal connected to the first input terminal, the second inverter including a second transistor having a second current driving capacity that is smaller than the first current driving capacity; and

an inversion circuit having a third output terminal connected to the first input terminal, the inversion circuit receiving an input signal having a second

amplitude that is smaller than the first amplitude, the input signal including a first input signal and a second input signal, the inversion circuit including a third transistor having a third current driving capacity that is smaller than the first current driving capacity and is larger than the second driving capacity.

20. A level shift circuit according to claim 19, wherein one of the first and second input signals is a one-shot pulse signal.